# Bridge-Type Integrated Hybrid DC Circuit Breakers

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***Abstract*-- The inclusion of a large number of controllable semiconductor devices in conventional hybrid dc circuit breakers (HCBs) may significantly increase the cost of an HVDC grid protection scheme. In an attempt to reduce this cost, this paper proposes the use of two novel topologies of bridge-type integrated HCBs (BT-ICBs). The two configurations are examined in detail, their operation sequences are established and a detailed parametric analysis is conducted. The total number of controllable semiconductor devices in a BT-ICB is assessed with the aid of selectivity studies and a comparison is made when conventional HCB and other ICB topologies are considered. It is shown that the proposed configurations employ 50 to more than 70% less controllable devices compared to conventional HCBs. The proposed BT-ICB topologies are tested in PSCAD/EMTDC using a four-terminal HVDC grid. Simulation results demonstrate the capability and effectiveness of the proposed solutions to isolate different types of dc faults at either a dc line, a converter terminal or a dc bus.**

***Index Terms*-- dc circuit breakers, HVDC grids, protection.**

## I. Introduction

VOLTAGE source converter (VSC) based HVDC grids will be instrumental to integrate large-scale renewable energy generation into electricity grids and to enable cross-border energy trading [1]. Presently, only regional multi-terminal VSC-HVDC systems are in operation or being constructed [2]-[4]. Major deployment of large HVDC grids still requires further advances in HVDC network protection.

Strategies for protecting HVDC grids rely on different devices. These may include ac circuit breakers (ACCBs), converters with fault blocking capability, and dc circuit breakers (DCCBs) [5]. ACCBs have been utilized for protecting point-to-point HVDC links. Even when the use of ACCBs for the protection of HVDC grids is also possible, de-energization of the whole dc grid for a lengthy period is required prior to the isolation of a dc fault due to the slow action of ACCBs [6], [7]. An alternative is to use VSCs based on full-bridge (FB) submodules with fault blocking capability [8]-[10]. An FB converter can be immediately blocked or controlled to reverse its dc voltage to suppress the dc fault current. However, an FB topology has more semiconductor devices, higher conduction losses and thus an increased cost than an equivalent half-bridge type VSC. Moreover, protection schemes for dc grids based on converter operation only will not be selective as all converters must be blocked until the dc fault is isolated.

Alternatively, the protection of HVDC networks connected to converters without fault blocking capability (*e.g.* half-bridge modular multi-level converter, HB-MMC) can also rely on the bypassing of converters and, hence, prevent the fault current contributed from both the capacitors within converters and the connected ac systems [11]-[13]. Reference [11] proposes the use of a double-thyristor unit connected in parallel with each submodule (SMs) of the HB-MMCs. Once a dc fault happens, this unit will turn on to bypass the SMs. The dc fault can be then converted into a balanced ac three-phase fault which can be isolated by ACCBs existing in the network. In [12], the double-thyristor units presented in [11] are connected to the ac terminal of each converter instead. This further reduces the $\frac{dv}{dt}$ stress across the double-thyristor units during normal operation and fully prevents the fault current from flowing through the diodes within SMs when a dc fault happens. In [13], a hybrid bypassing approach is proposed. In the event of a dc fault, a bypass circuit can also be created by triggering the thyristor units and then use DCCBs combined with only very few IGBTs and fast mechanical switches to isolate the dc fault.

The methods proposed in [11]-[13] have been examined using point-to-point links and their effectiveness isolating dc faults using relatively low-cost devices (*e.g.* mechanical switches) has been documented. However, if these methods are used for HVDC grid protection, the whole dc grid would still need to be de-energized as the MMCs would be bypassed for a relatively long period (*e.g.* >20 ms) until the dc fault current becomes zero. The recovery of an MMC station from a bypassing operation could also be slow and would cause disturbances to both ac and dc systems.

A more suitable approach is to install DCCBs at both ends of each dc line to selectively protect the dc grid. Different alternatives have been proposed in the open literature, including mechanical resonant circuit breakers (MRCBs) [14], [15], full solid-state circuit breakers (FSCBs) [16], [17] and hybrid DC circuit breakers (HCBs) [18], [19]. A typical MRCB has a resonant LC circuit that enables zero-crossings following a fault. This way, the fault can be interrupted; however, the speed of operation is slow – around 60 ms [15]. This time can be reduced to 8-10 ms by adding a charging unit in parallel with the capacitor, but this still could be too slow to interrupt a fast-rising dc fault current [20], [21].

FSCBs can block dc fault currents within 1 ms without any arc. However, these devices employ hundreds of semiconductor switches in series and, as a result, exhibit unacceptably high conduction losses. Conduction losses can be around 30% of the losses of an equivalently rated converter [22]. Instead, HCBs featuring low conduction losses and a fast speed of operation (2-3 ms) have been developed. Different topologies have been proposed, but in general they consist of a low-loss bypass branch and a bidirectional main breaker (BMB) associated with surge arresters. Current flows through the bypass branch during normal operation and is commutated to the BMB for current interruption when a dc fault occurs. The major shortcoming of an HCB is its high investment cost. Its BMB contains hundreds

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of anti-series connected controllable semiconductor devices which are turned off to interrupt currents of high magnitudes.

Given that the cost for fully protecting an HVDC grid will be significant as multiple DCCBs are needed, it is essential to restrict the use of controllable switches to make dc protection more cost-effective. The use of unidirectional HCBs can reduce the number of controllable semiconductors by half at the expense of only being capable of interrupting currents in the forward direction [23], [24]. An H-bridge based HCB can relieve this shortcoming as it can block current bidirectionally with similar number of controllable switches as a unidirectional HCB [25]. However, such device is still defenseless to internal bus faults. Alternatively, different HVDC grid topologies have been designed to reduce the number of HCBs [26]. Other methods aim to reduce the HCB cost by either reducing the size of surge arresters or using advanced current limiters [27], [28].

Despite their advantages, the discussed DCCB topologies may not minimize the number of controllable semiconductor devices. If it is desired to protect a dc grid where dc buses are connected to multiple nodes (>2), a cost-effective way is to deploy an integrated HCB (ICB) device at each dc bus instead of using several DCCBs. This idea is illustrated with the schematics shown in Fig. 1, where an ICB will share the use of semiconductor devices. It is worth mentioning that there may be different topologies for an ICB and, thus, Fig. 1(b) represents a generic illustration of the concept.

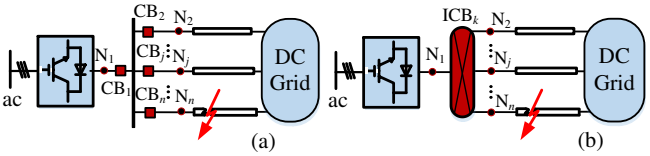



Fig. 1. HVDC grid protected by (a) HCBs; (b) ICBs.

Different ICB topologies have been proposed in the literature to reduce the total semiconductor count. This has been achieved by sharing: (i) one main breaker (MB) with additional thyristors and grounding circuits [29]; (ii) several MBs with smaller rating [30], [31], [32]; or (iii) one MB plus extra bypass branches [33], [34]. The approach in (i) requires many thyristors and extra grounding points for its operation, which may be undesirable. Conversely, (ii) reduces the number of controllable semiconductor devices by 25-50%, with the number of connected nodes increasing from three to a large number. Savings are apparent as the number of nodes increases. In contrast, solution (iii) can potentially reduce the number of controllable devices for a wide range of connected nodes as a single BMB is needed only [33]. Further reduction is achieved by replacing the BMB with a unidirectional main breaker (UMB) plus two more bypass branches [34]. However, such a structure becomes defenseless to internal bus faults and will take longer time to isolate a fault if the pre-fault currents in the bypass branches flow in a backward direction.

To minimize the use of controllable semiconductors while protecting dc grids from faults at dc lines, converter terminal and dc buses, this paper proposes a bridge-type ICB (BT-ICB) based on [30], [33] . The key idea is to share one bridge-type MB (BTMB) with modified bypass branches to protect multiple dc nodes. Two new different BT-ICBs topologies are developed. Their operation and control principle for different fault events are provided and a detailed parametric analysis is performed. Sensitivity studies are carried out to estimate the required number of controllable devices and a comparison with other solutions is made. The effectiveness of using BT-ICBs to isolate dc faults is assessed by simulation studies in PSCAD.

## II. Integrated Hybrid DC Circuit Breaker

### A. Conventional HCB

Fig. 2 shows a conventional HCB. It has a bypass branch and a BMB with surge arresters [18]. The bypass branch consists of a load commutation switch (LCS) and a mechanical ultrafast disconnector (UFD). Current flows through the LCS and the UFD during normal operation. Once a tripping signal is received, the LCS will immediately block to commutate the fault current into the BMB. The UFD can then open following a time delay of several milliseconds. A current limiting reactor (CLR) is used to mitigate the rate of current rise in this period. After the UFD fully opens, the BMB will trip to interrupt the fault current and the fault energy will be absorbed by the surge arresters. The residual current breaker (RCB) will also open after the fault current is reduced to zero.

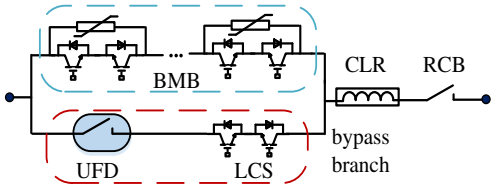



Fig. 2. Configuration of a HCB.

### B. Topologies of BT-ICBs

Fig. 3 shows the first proposed topology of a BT-ICB. It includes a shared BTMB connected between two internal dc buses A and B, and 2×($n$ − 1) bypass branches with UFDs and modified LCSs (further detail is given in the next paragraph). The value of $n$ is determined by the number of connected nodes ($N_1$, $N_2$…$N_n$). Connecting a new node to the ICB would only require two additional bypass branches.

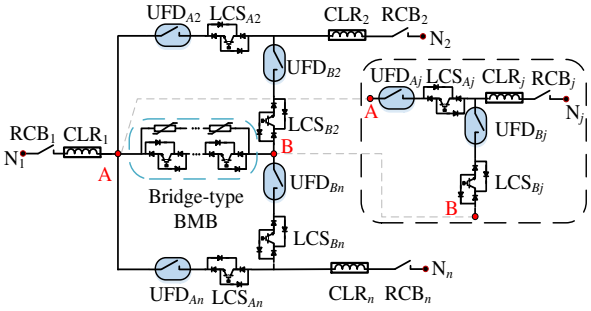



Fig. 3. BT-ICB.

The BTMB consists of series-connected semiconductor based units with surge arresters. Each unit has a single IGBT ($S_1$) and four diodes ($D_1$ to $D_4$) connected in a bridge configuration, as shown in Figs. 4(a) and 4(b). Current flows through $D_3$, $S_1$ and $D_2$ in a forward direction and through $D_1$, $S_1$ and $D_4$ in a backward direction. $S_1$ can be turned off when a tripping signal is received so that a fault current is interrupted. It should be highlighted that the bidirectional blocking bridge circuit employing one IGBT and four diodes has been previously used in other power electronic applications, such as matrix converters. However, the application of such circuit on the configuration in [33] to create the proposed BT-ICB topology is relevant as it drastically reduces the number of IGBTs.

Since diodes cost much less than IGBTs (≈10 times [35]), this configuration is cheaper than one employing IGBT units connected in anti-series to block fault bidirectionally (see Fig. 4(c) and 4(d)). The need for IGBT drivers will be also reduced by 50%. For these reasons, the bridge-type configuration is also adopted for the LCSs shown in Fig. 3.

It is worth to note that to practically connect the semiconductors of BTMBs in series, a resistor-capacitor-diode (RCD) snubber circuit can be embedded within each semiconductor-based unit as shown in Fig. 5. The RCD snubber circuits are used to ensure the equal voltage distribution of semiconductor-based units during current breaking. This is similar to the implementation of conventional HCBs [18] where the same RCD snubber circuits are connected in parallel with IGBT units.

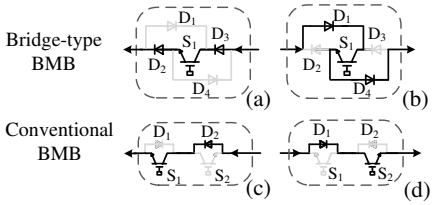



Fig. 4. Bridge-type BMB (and LCS) current conduction in (a) forward and (b) backward directions. Conventional BMB current conduction in (c) forward and (d) backward directions.

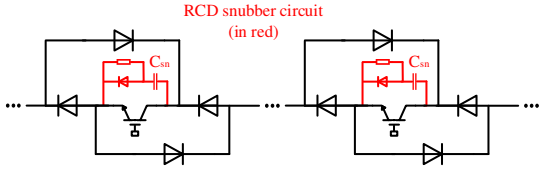



Fig.5. RCD snubber circuit (in red).

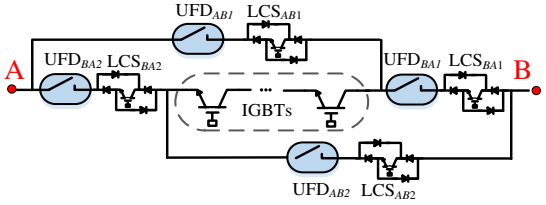



Fig. 6. Alternative for the BTMB arrangement.

An alternative configuration for the BTMB is shown in Fig. 6. Extra bypass branches are connected as an H-bridge between nodes A and B for current commutation and, hence, this eliminates the need of diodes for fault blocking in those IGBT units. The use of bypass branches instead of diodes may facilitate the maintenance of a BT-ICB.

A BT-ICB employing the BTMB shown in Figs. 4(a) and 4(b) is denoted Type 1 BT-ICB (BT-ICB$_{typ1}$) for the remainder of the paper; conversely, a BT-ICB using a BTMB based on the structure in Fig. 6 is called Type 2 BT-ICB (BT-ICB$_{typ2}$).

The total number of bypass branches (including UFDs and LCSs) of BT-ICB$_{typ2}$ is given by $2\times(n + 1)$, where $n$ is the number of connected nodes. Instead, BT-ICB$_{typ1}$ contains $2\times(n - 1)$ bypass branches. Therefore, BT-ICB$_{typ2}$ has 4 more additional bypass branches as these are used to replace the 4 diode bridges from the MB of BT-ICB$_{typ1}$.

Fig. 7 provides a schematic view of BT-ICB$_{typ2}$. The difference between BT-ICB$_{typ2}$ and BT-ICB$_{typ1}$ is highlighted inside the red box, where the 4 additional bypass branches are used to replace the 4 diode bridges from the MB of BT-ICB$_{typ1}$. The remaining parts of the circuit (outside the red box) are similar for both topologies.

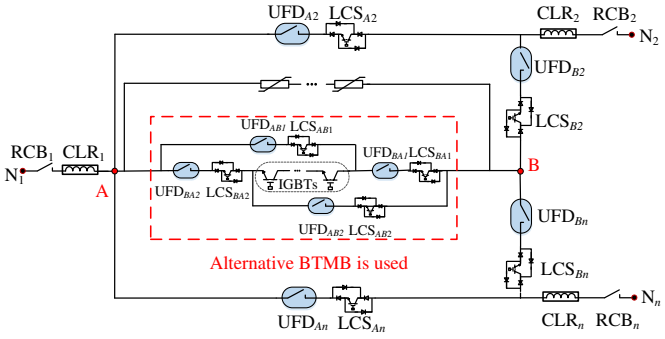



Fig. 7. Diagram of BT-ICB$_{typ2}$.

The practical design of the proposed topologies is not expected to be much more complex than for conventional HCBs. Compared to HCBs, BT-ICBs have extra LCSs and UFDs to reduce the use of MBs based on semiconductor devices. The bridge type bidirectional switch within the LCSs can be designed as individual stacks (one IGBT and four diodes per stack). If it is desired to increase the current and voltage ratings of the LCSs, additional stacks can be placed in parallel or in series. This process is similar to the implementation of the anti-series connected circuits used in HCBs. Although the inclusion of extra LCSs would require additional cooling systems, the size of each cooling system can be reduced as the power losses of the proposed DCCBs are lower than for conventional HCBs. The extra UFDs are mechanical components. This facilitates the maintenance of the proposed BT-ICBs topologies when compared to HCBs – which require extra semiconductor units to build the additional MBs.

**Note:** The BT-ICB variant presented in [33] can be obtained when the IGBTs are connected in anti-series. A schematic diagram for an anti-series connected ICB (denoted hereafter AS-ICB) is provided in Fig. 8. The assessment of the BT-ICB configurations (i.e. BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$) proposed in this paper includes a comparison with the AS-ICB topology in Section III-B.

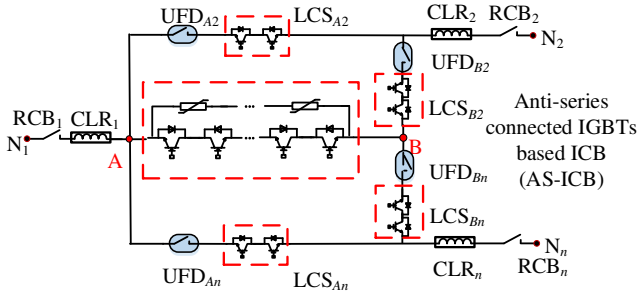



Fig. 8. Schematic diagram of an AS-ICB.

### C. *Operation principle of BT-ICB$_{typ1}$*

The operating sequence of a BT-ICB$_{typ1}$ for blocking a dc line fault is shown using the simplified diagram in Fig. 9. It is assumed that a converter is connected to node $N_1$ and dc transmission lines are connected to nodes $N_2 \ldots N_j \ldots N_n$.

From $t_0$ to $t_1$, BT-ICB$_{typ1}$ receives a tripping signal to block a fault at $N_j$. The LCSs of all bypass branches coordinate to commutate the current to the BTMB. The bypass branch connected to the faulty node linked to A will open its LCS ($LCS_{Aj}$), while the one linked to B will stay closed ($LCS_{Bj}$). For the bypass branches connected to the healthy nodes, the LCSs linked to B will open ($LCS_{B\beta}$, $\beta \in \{2, n\}$, $\beta \neq j$, where $\beta$ represents each node) and those linked to A will remain closed

($LCS_{A\beta}$, $\beta \in \{2, n\}, \beta \neq j$). The fault current will then only flow through the BTMB in a backward direction (via $D_1$, $S_1$ and $D_4$ as shown in Fig. 4(b)).

From $t_1$ to $t_2$, the mechanical UFDs associated to the opened LCSs will also open ($UFD_{A\beta}$, $\beta \in \{2, n\}$, $\beta \neq j$). This takes several milliseconds and its operation is similar to that of conventional HCBs. It is also worth noticing that since the UFDs are mechanical components, their opening time could be different even if the devices are identical. However, the correct operation of the BT-ICB will be achieved as long as the BTMB is opened only after all the corresponding UFDs fully open. This does not require a specific coordination of the UFDs.

At $t_2$ the BTMB immediately interrupts the fault current by turning off the IGBT in each semiconductor-based unit. The fault current will drop and the fault energy will be fully absorbed by the associated surge arresters at $t_3$. At this point, the fault is isolated. From $t_3$ onwards, the RCB at $N_j$ ($RCB_j$) is opened to disconnect the faulty circuit. Once this is done, the remaining components can then re-close to protect the remainder of dc network. If a fault occurs at any other dc line, the operation sequence described above will be repeated but for fault isolation at the other line.

If it is desired to isolate a fault at the converter side (connected to $N_1$), the operating sequence before $t_2$ is slightly different. This is shown in Fig. 10. All LCSs linked to A will open while those connected to B will stay closed. The fault current will then only flow through the BTMB in a forward direction (through $D_2$, $S_1$ and $D_3$, see Fig. 4(a)). The UFDs connected to A will then open followed by the turn-off of the BTMB. Similarly, $RCB_1$ can then open to isolate the converter from the grid side (nodes $N_2$ to $N_n$) and all other components can re-close to protect the remaining dc lines. Note that as $N_1$ is connected to the converter, it can be blocked and use ACCBs to interrupt the fault current contributed from the converter side. This would be similar to a protection scheme based on conventional HCBs (*e.g.* a fault at $N_1$ in Fig. 1 (a)).

A $BT\text{-}ICB_{typ1}$ can also block an internal fault at both buses A and B as its BTMB can interrupt fault current bidirectionally. The operating sequence for blocking a fault at A is the same as that for isolating a fault at $N_1$ during $t_0$ to $t_3$. The only difference is that the BTMB alongside the LCSs and UFDs linked to A must be kept open after the fault is blocked to isolate A from the grid side. Similarly, for blocking a fault at B, the LCSs and UFDs linked to B must open, followed by the turn-off of the BTMB, as shown in Fig. 11.

The total operating speed of a $BT\text{-}ICB_{typ1}$ is the same compared to that of conventional HCBs since the LCSs in a BT-ICB coordinate to open at the same time as the UFDs; hence no extra delay is added to the operation. Consequently, if the same CLRs are deployed at the nodes and if the circuit breakers resistances are neglected, a $BT\text{-}ICB_{typ1}$ can interrupt a dc current of a similar magnitude as an HCB with much less controllable semiconductors. An extra advantage of using $BT\text{-}ICB_{typ1}$ is that currents are still transmitting through the nodes even at the occurrence of an internal bus fault. This would be impossible if the bus is protected by conventional HCBs as those at the faulty bus must be opened and, as a result, current will stop flowing through the connected nodes.

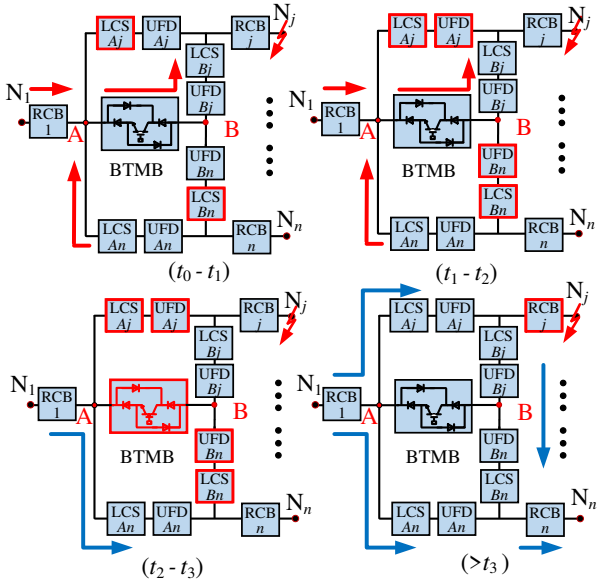



Fig. 9. Operating sequence for blocking a dc line fault using $BT\text{-}ICB_{typ1}$.

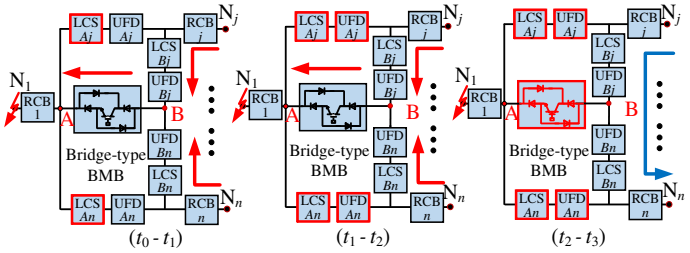



Fig. 10. Operating sequence for blocking a converter side fault using $BT\text{-}ICB_{typ1}$.

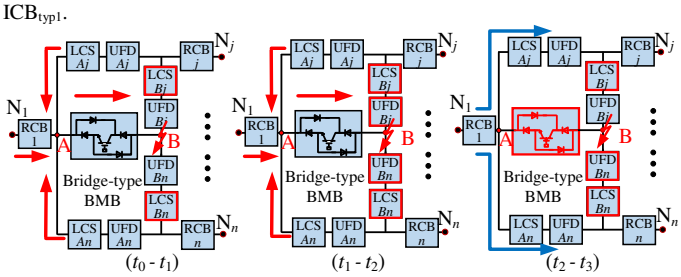



Fig. 11. Operating sequence for blocking a fault at bus B using $BT\text{-}ICB_{typ1}$.

### *D. Operation principle of BT-ICB$_{typ2}$*

The operating sequence for $BT\text{-}ICB_{typ2}$ is similar to that of $BT\text{-}ICB_{typ1}$ but requires additional coordination due to the extra bypass branches. Fig. 12 shows the operation of $BT\text{-}ICB_{typ2}$ when a fault is applied at $N_j$. Prior to $t_2$, upon detection of a fault, the LCSs at the extra bypass branches in the forward direction ($LCS_{BA1}$ and $LCS_{BA2}$) should be opened together with $LCS_{Aj}$ and $LCS_{B\beta}$ ($\beta \in \{1, n\}$, $\beta \neq j$). Any other LCS should be kept closed. The fault can then be commutated to the string of IGBT units. The UFDs associated with the opened LCSs will then turn off. After $t_2$, the fault current will be interrupted by tripping the string of IGBTs. The fault will be isolated after the fault energy is absorbed by the surge arresters. All components can be restored after the opening of $RCB_j$.

The operating sequence when a $BT\text{-}ICB_{typ2}$ is used to block a fault at the converter side ($N_1$) is given in Fig. 13. Prior to $t_2$, the LCSs at the extra bypass branches in the backward direction ($LCS_{AB1}$, $LCS_{AB2}$) and all the LCSs connected to A will open to

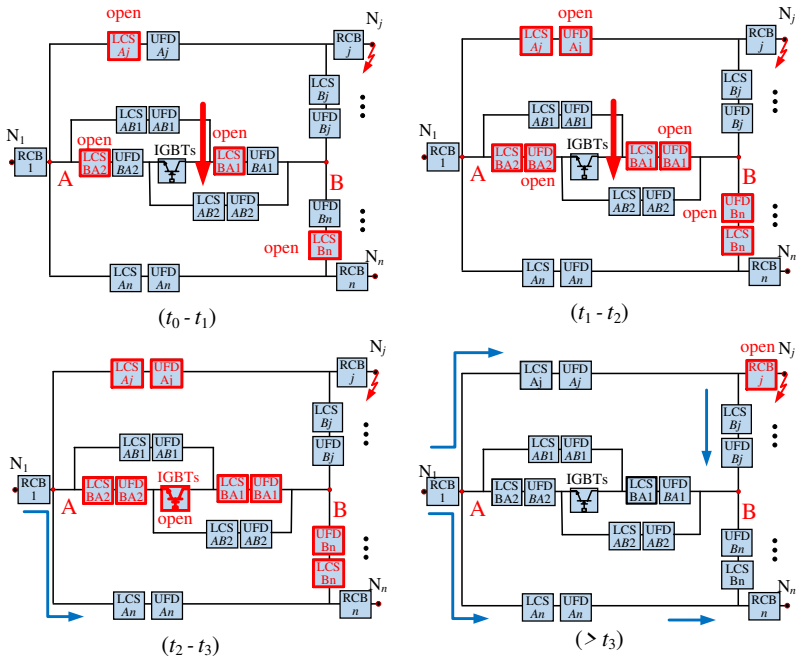



Fig. 12. Operating sequence for blocking a fault at dc line using BT-ICB$_{typ2}$.

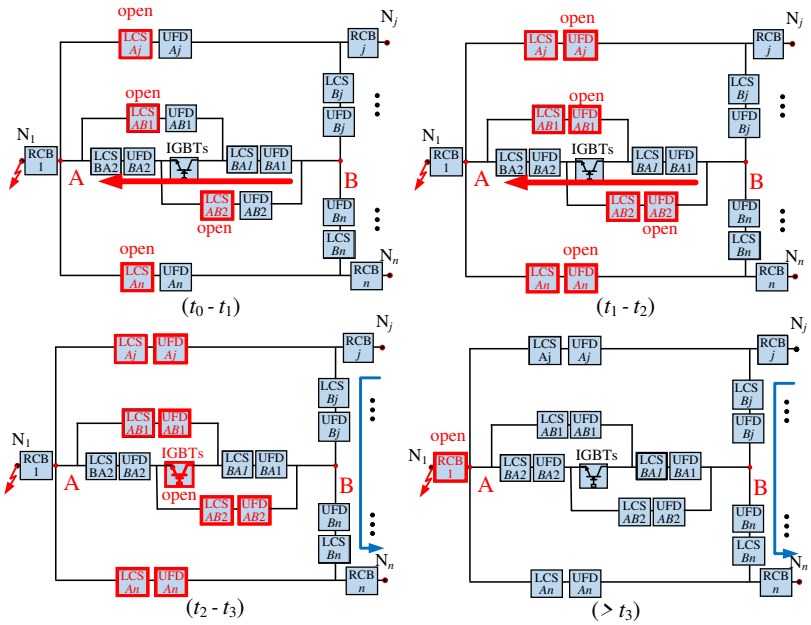



Fig. 13. Use of BT-ICB$_{typ2}$ for blocking a converter side fault.

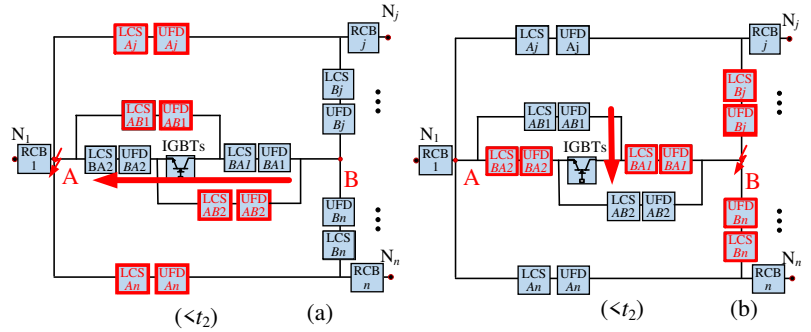



Fig. 14. Use of BT-ICB$_{typ2}$ for blocking a bus fault at (a): A; (b): B.

commutate the fault current to the string of IGBTs. After $t_2$, the string of IGBTs turn off to interrupt the current. Once RCB$_1$ is opened, the remaining open components can be reclosed.

The difference between using BT-ICB$_{typ2}$ or BT-ICB$_{typ1}$ to isolate internal bus faults at A and B occurs prior to $t_2$. LCS$_{AB1}$ and LCS$_{AB2}$ of BT-ICB$_{typ2}$ must be also opened to isolate a fault

at A (see Fig. 14(a)), while $LCS_{BA1}$ and $LCS_{BA2}$ must be opened to isolate a fault at B (see Fig. 14(b)). In BT-$ICB_{typ1}$, which has less bypass branches, the current is commutated by the diodes instead. The operation of both devices after $t_2$ is similar.

The operating sequence of BT-$ICB_{typ2}$ for different fault events is summarized in Table I. In general, when a dc fault takes place, the LCSs that are required to act will always trip first to commutate currents flowing into the string of IGBTs (Step 1). The UFDs on the same bypass branches as those tripped LCSs will then open (Step 2). After that, the string of IGBTs will open immediately to block the fault (Step 3). For a dc line or a converter fault, the RCB at the faulty circuit can open and, hence, other components can be restored (Step 4). For a bus fault at A or B, the opened components should remain open to isolate the bus fault.

TABLE I. SUMMARY OF THE OPERATING SEQUENCE OF BT-ICBTYP2.

| | Dc line fault (at $N_j$) | Converter fault (at $N_1$) | BUS A fault (at A) | BUS B fault (at B) |
|---|---|---|---|---|
| Step 1 | Open $LCS_{BA1}$, $LCS_{BA2}$, $LCS_{Aj}$ and $LCS_{Bn}$ | Open $LCS_{AB1}$, $LCS_{AB2}$, $LCS_{Aj}$ and $LCSA_n$ | Open $LCS_{BA1}$, $LCS_{BA2}$, $LCS_{Aj}$ and $LCS_{An}$ | Open $LCS_{AB1}$, $LCS_{AB2}$, $LCS_{Bj}$ and $LCS_{Bn}$ |
| Step 2 | Open $UFD_{BA1}$ $UFD_{BA2}$, $UFD_{Aj}$ and $UFD_{Bn}$ | Open $UFD_{AB1}$, $UFD_{AB2}$, $UFD_{Aj}$ and $UFDA_n$ | Open $UFD_{BA1}$, $UFD_{BA2}$, $UFD_{Aj}$ and $UFD_{An}$ | Open $UFD_{AB1}$, $UFD_{AB2}$, $UFD_{Bj}$ and $UFD_{Bn}$ |
| Step 3 | Open IGBTs | Open IGBTs | Open IGBTs | Open IGBTs |
| Step 4 | Open $RCB_j$, restore other components | Open $RCB_1$, restore other components | N/A | N/A |

## III. ANALYSIS AND DESIGN OF BT-ICBS

### A. Parametric Analysis of BT-ICBs

A BT-ICB should interrupt every fault current. Thus, the voltage and current rating of its components should consider not only faults at the dc nodes connected to lines or converters, but also faults at internal buses, which would lead to a maximum fault current flow through the BT-ICB.

The most severe fault at a dc line or converter terminal will be a solid fault at a node of the BT-ICB (*e.g.* $N_j$). It is assumed that the BT-ICB detects the fault when fault current $i_j(t)$ is 1.5 times the rated current and the LCSs will immediately coordinate to commutate current to the BTMB. The value of the fault current at $t_1$ is approximately:

$$I_{j,t_1} = 1.5I_{rated} \tag{1}$$

since the turn-off speed of LCSs is extremely fast (only a fraction of a millisecond) [36]. The fault current will keep rising through the BTMB during the delay caused by the opening of UFDs (during $t_1$ to $t_2$, about 2 ms [37]).

Fig. 15 shows an equivalent circuit from $t_1$ to $t_2$. $L_1 \dots L_n$ represent the CLRs' inductances. $L_{eq1} \dots L_{eqn}$ and $C_{eq1} \dots C_{eqn}$ are the inductances and capacitances of the nearby connected dc network. The resistance of the bypass branches is negligible as it is much smaller than the equivalent resistance ($R_{MB1}$ for BT-$ICB_{typ1}$ and $R_{MB2}$ for BT-$ICB_{typ2}$) and the forward voltage drop of semiconductors of the BTMB ($U_{fwd1}$ for BT-$ICB_{typ1}$ and $U_{fwd2}$ for BT-$ICB_{typ2}$).

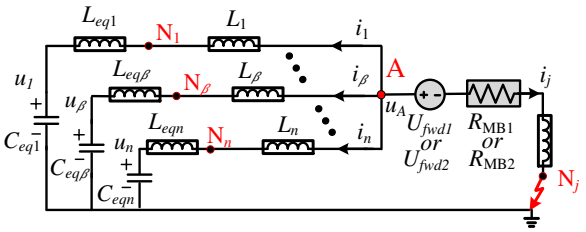



Fig. 15. Equivalent circuit for fault at node *j*.

If BT-$ICB_{typ1}$ is used, the voltage at node A $u_A(t)$ is:

$$u_A(t) - U_{fwd1} = R_{\mathrm{MB1}} i_j(t) + L_{\mathrm{j}} \frac{di_j(t)}{dt} \tag{2}$$

The voltage across each healthy circuit can be represented as:

$$u_A(t) - u_\beta(t) = (L_{\mathrm{j}} + L_{eqj}) \frac{di_\beta(t)}{dt};\ \beta \in \{1, n\}, \beta \neq j \tag{3}$$

where $\beta$ is an integer from 1 to $n$ to represent the healthy circuit, and $j$ is the node where a fault is applied.

The fault current (before interruption) will only reach its maximum value if all connected dc systems keep operating at approximately a maximum dc voltage ($U_{rated}$) in a short period:

$$u_\beta(t) = U_{rated};\ \beta \in \{1, n\}, \beta \neq j \tag{4}$$

Equation (3) can then be rewritten as:

$$u_A(t) - U_{fwd1} = -L_{\mathrm{hlthy}} \frac{di_j(t)}{dt} + U_{rated} \tag{5}$$

where $L_{\mathrm{hlthy}}$ is the equivalent inductance of healthy circuits, defined as

$$\frac{1}{L_{\mathrm{hlthy}}} = \sum_{\substack{\beta=1 \\ \beta \neq j}}^{n-1} \frac{1}{(L_{eq\beta} + L_\beta)} \tag{6}$$

Substituting (5) into (2) gives:

$$R_{\mathrm{MB1}} i_j(t) + \left(L_{\mathrm{j}} + L_{\mathrm{hlthy}}\right) \frac{di_j(t)}{dt} = U_{rated} - U_{fwd1} \tag{7}$$

The expression of fault current $i_j(t)$ is then obtained as:

$$i_j(t) = 1.5I_{rated} + \frac{U_{rated} - U_{fwd1}}{R_{\mathrm{BMB}}} \times \left[1 - e^{\frac{-R_{\mathrm{MB1}}}{L_{\mathrm{hlthy}} + L_{\mathrm{j}}} \times (t - t_1)}\right] \tag{8}$$

If BT-$ICB_{typ2}$ is used instead, the fault is given by:

$$i_j(t) = 1.5I_{rated} + \frac{U_{rated} - U_{fwd2}}{R_{\mathrm{UMB}}} \times \left[1 - e^{\frac{-R_{\mathrm{MB2}}}{L_{\mathrm{hlthy}} + L_{\mathrm{j}}} \times (t - t_1)}\right] \tag{9}$$

Both (8) and (9) are further simplified if the sum of inductances is much greater than the resistances of the BTMBs ($L_{\mathrm{j}} + L_{\mathrm{hlthy}}$)$R_{\mathrm{MB1}}$ and $R_{\mathrm{MB2}}$) and if $U_{fwd1}$ and $U_{fwd2}$ are ignored as they are much smaller than $U_{rated}$:

$$i_j(t) = 1.5I_{rated} + \frac{U_{rated}}{L_{\mathrm{j}} + L_{\mathrm{hlthy}}} \times (t - t_1) \tag{10}$$

Therefore, the maximum current flow through both types of BT-ICBs for interruption at $t_2$ is:

$$I_{MB,nodeflt} = 1.5I_{rated} + \frac{U_{rated}}{L_{\mathrm{j}} + L_{\mathrm{hlthy}}} \times (t_2 - t_1) \tag{11}$$

The maximum voltage across the BTMBs is determined by the level of voltage protection of their associated surge arresters –typically selected as $1.5U_{rated}$ [22]. It should be noticed that the voltage across the opened UFDs in the bypass branches are the same as the voltage of the BTMB when the BTMB blocks the current. The voltage drop across the opened LCSs is negligible when compared to the voltages across opened UFDs. Therefore, the voltage rating of UFDs should also be selected as 1.5 times the dc system voltage. The maximum energy absorbed will then be:

$$E_{MB,nodeflt} = 1.5U_{rated} \times I_{MB,nodeflt} \frac{(t_3 - t_2)}{2} \tag{12}$$

where $t_3$ is the instant when the current through the surge arresters drops to zero.

The LCSs in the BT-ICBs' bypass branches should have a similar current rating as their BTMBs as the same rate of fault current (before interruption) will flow through one of the bypass branches connected to the faulty node (*e.g.* $LCS_{Bj}$ in Fig. 11). That is,

$$I_{\mathrm{LCS},nodeflt} = I_{MB,nodeflt} \tag{13}$$

However, the voltage rating of the LCSs is much smaller, as this only needs to exceed the on-state voltage of the BTMBs if the resistance of other LCSs is ignored. Therefore,

$$\begin{cases} U_{\mathrm{LCS},BT1,nodeflt} = I_{MB,nodeflt} \times R_{MB1} + U_{fwd1} \\ U_{\mathrm{LCS},BT2,nodeflt} = I_{MB,nodeflt} \times R_{MB2} + U_{fwd2} \end{cases} \tag{14}$$

The most severe bus fault will be a solid fault at B as this maximizes the current $i_B$ flowing through the BTMB (see Fig. 16). Similarly, assuming the BT-ICB detects a fault at B when the sum of node currents is 1.5 times of the rated current, $i_B$ at $t_1$ ($I_{B,t_1}$) will approximately be:

$$I_{B,t_1} = -\sum_{\beta=1}^{n} I_{\beta,t_1} = 1.5 I_{rated} \tag{15}$$

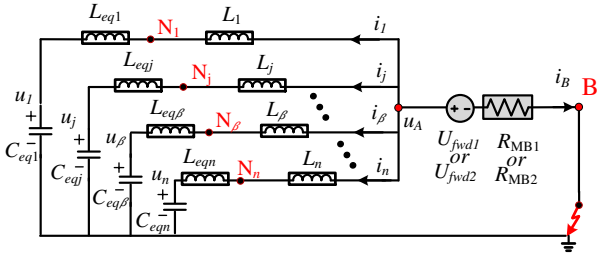



Fig. 16. Equivalent circuit for a bus fault.

Applying the same analysis for the dc network fault, a simplified expression for $i_B$ can be obtained as

$$i_B(t) = 1.5 I_{rated} + \frac{U_{rated}}{L_{\mathrm{hlthyB}}} \times (t - t_1) \tag{16}$$

where $L_{\mathrm{hlthyB}}$ is the total inductance of the healthy circuits in event of a bus fault. This is given by

$$\frac{1}{L_{\mathrm{hlthyB}}} = \sum_{\beta=1}^{n} \frac{1}{(L_{eq\beta})} \tag{17}$$

$L_{\mathrm{hlthyB}}$ is smaller than ($L_{\mathrm{hlthy}}$+$L_j$) and hence $i_B(t)$ increases at a higher rate than $i_j(t)$. Thus, to successfully interrupt the fault current at $t_2$, the BTMB should withstand a current

$$I_{MB,busflt} = 1.5 I_{rated} + \frac{U_{rated}}{L_{\mathrm{hlthyB}}} \times (t_2 - t_1). \tag{18}$$

The maximum energy absorbed by the associated surge arrester for a bus fault is given as

$$E_{MB,busflt} = 1.5 U_{rated} \times I_{MB,busflt} \frac{(t_{itp} - t_2)}{2} \tag{19}$$

The maximum current of an LCS in closed state is the same as the connected node current:

$$I_{LCS,busflt} = I_{\beta,t1} + \frac{U_{rated}}{L_\beta} \times (t_2 - t_1) \tag{20}$$

where $I_{\beta,t1}$ is the current flowing through node $\beta$ at $t_1$. As $L_\beta$ is larger than $L_{\mathrm{hlthyB}}$, the rise of currents in LCSs will be slower than the rise of current in the BTMB.

The voltage rating of the LCSs is then given as:

$$\begin{cases} U_{\mathrm{LCS},BT1,busflt} = I_{MB,busflt} \times R_{MB1} \\ U_{\mathrm{LCS},BT2,busflt} = I_{MB,busflt} \times R_{MB2} \end{cases} \tag{21}$$

### *B. Comparison of different DCCB topologies*

This section provides an estimation of the total IGBTs when different topologies of DCCBs are used—aiming to reduce the total number of IGBTs of a protection scheme.

The analysis in Section III-A shows that a bus fault will incur higher current than a dc line fault in the BTMB. Thus, an adequate number of IGBTs should be included in the BTMBs to withstand $I_{MB,busflt}$ as defined by (18). The current in LCSs $I_{\mathrm{LCS},busflt}$ will be smaller than $I_{MB,busflt}$; however, if the inductance of the CLRs is extremely small, $I_{\mathrm{LCS},busflt}$ will be approximately equal to $I_{MB,busflt}$.

The total required IGBTs of a $\text{BT-ICB}_{\text{typ1}}$ (including both in LCSs and the BTMB) can be obtained as:

$$M_{IGBT,BT1} = \mathrm{ceil}\left(\frac{I_{MB,busflt}}{I_{igbt}}\right) \times \left[\mathrm{ceil}\left(\frac{1.5U_{rated}}{U_{igbt}}\right) + 2(n-1) \times \mathrm{ceil}\left(\frac{U_{\mathrm{LCS},BT1,busflt}}{U_{igbt}}\right)\right]. \tag{22}$$

For $\text{BT-ICB}_{\text{typ2}}$, this is given by

$$M_{IGBT,BT2} = \mathrm{ceil}\left(\frac{I_{MB,busflt}}{I_{igbt}}\right) \times \left[\mathrm{ceil}\left(\frac{1.5U_{rated}}{U_{igbt}}\right) + 2(n+1) \times \mathrm{ceil}\left(\frac{U_{\mathrm{LCS},U,busflt}}{U_{igbt}}\right)\right]. \tag{23}$$

where function "ceil" rounds each element to the nearest integer greater than or equal to that element. $U_{igbt}$ and $I_{igbt}$ are the transient peak voltage and collector current of a single IGBT. Equations (22) and (23) illustrate that additional IGBTs will be connected in parallel to increase the breaker's current rating and in series to increase the voltage rating.

If conventional HCBs are used, at least $n$ HCBs are needed to protect a bus connected to $n$ nodes. In this case, the total number of IGBTs is given by

$$M_{IGBT,HCBs} = 2 \times \sum_{\beta=1}^{n} \left[\mathrm{ceil}\left(\frac{I_{MB,HCB\beta}}{I_{igbt}}\right) \times \mathrm{ceil}\left(\frac{1.5U_{rated}}{U_{igbt}}\right) + \mathrm{ceil}\left(\frac{1.5I_{rated}}{I_{igbt}}\right) \times \mathrm{ceil}\left(\frac{U_{\mathrm{LCS},HCB\beta}}{U_{igbt}}\right)\right] \tag{24}$$

where $I_{MB,HCB\beta}$ is the peak current flowing through one HCB and $U_{\mathrm{LCS},HCB\beta}$ is the maximum voltage across its LCS. $I_{MB,HCBk}$ is only reached at the occurrence of a bus fault. Using the analysis carried out in Section III-A for the HCBs, $I_{MB,HCB\beta}$ for each single HCB can be expressed as:

$$I_{MB,HCB\beta} = 1.5 I_{rated} + \frac{U_{rated}}{L_\beta} \times (t_2 - t_1) \tag{25}$$

$U_{\mathrm{LCS},HCB\beta}$ is then given as:

$$U_{\mathrm{LCS},HCB\beta} = I_{MB,HCB\beta} \times R_{HCBMB} + U_{fwdHCB} \tag{26}$$

where $R_{HCBMB}$ and $U_{fwdHCB}$ are the equivalent resistance and forward voltage drop of the MB of an HCB.

Equation (24) shows that if HCBs are used, the number of IGBTs in the MBs will increase when more nodes are connected, although the size of their LCSs is smaller compared to those of a BT-ICB.

For completeness, the number of IGBTs for the ICB approach based in (iii) discussed in the Section I, which can also block faults at all nodes and internal buses, is assessed. This corresponds to the AS-ICB topology given by Fig. 8—based on anti-series connected IGBTs [33]. The total number of IGBTs for an AS-ICB is given by

$$M_{IGBT,AS} = 2 \times \mathrm{ceil}\left(\frac{I_{MB,busflt}}{I_{igbt}}\right) \times \left[\mathrm{ceil}\left(\frac{1.5U_{rated}}{U_{igbt}}\right) + 2(n-1) \times \mathrm{ceil}\left(\frac{U_{\mathrm{LCS},AS,busflt}}{U_{igbt}}\right)\right] \tag{27}$$

Its peak current will be approximately equal to $I_{MB,busflt}$ but the voltage rating of the LCSs ($U_{\mathrm{LCS},AS,busflt}$) will be slightly different due to the use of a different resistance ($R_{ASMB}$) and forward voltage drop ($U_{fwdAS}$). This is given by:

$$U_{\mathrm{LCS},AS\beta} = I_{MB,bus\beta} \times R_{ASMB} + U_{fwdAS} \tag{28}$$

A study to compare the number of IGBTs used in all approaches is performed. IGBT module 5SNA 3000K452300s is used, which can withstand a voltage of 4.5 kV and a peak current of 6 kA in transient conditions [38]. The DCCBs are initially rated at 400 kV and 1.5 kA. It is assumed that all terminal inductances are 0.12 H ($L_{eq\beta} + L_\beta = 0.12$ H, $\beta \in \{1, n\}$) and that UFDs have an operating speed of ms [37].

Fig. 17 shows the number of IGBTs for different DCCBs as a function of connected dc nodes. If conventional HCBs are used, the highest number of IGBTs is required. For example, when considering three nodes, a BT-ICB$_{typ1}$ employs 65.8% less IGBTs (552) when compared to those used by HCBs (1614). Similarly, BT-ICB$_{typ2}$ employs 63.8% less IGBTs (584) compared to HCBs. An AS-ICB reduces the number of IGTBs by 31.6% (1104). Therefore, BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ also reduce the total number of IGBTs by 34.2% and 32.2% compared to the AS-ICB. This is attributed to the anti-series connected IGBT units of the AS-ICB. BT-ICB$_{typ2}$ has 32 more IGBTs than BT-ICB$_{typ1}$ due to its additional bypass branches.

Fig. 17 also shows that the number of IGBTs increases proportionally with the number of nodes if HCBs are used. In other words, a new HCB will be added if a new dc node is connected. The relationship between the number of IGBTs against the number of nodes for BT-ICBs and AS-ICBs is almost piecewise linear. However, when reaching a certain number of connected dc nodes when ICBs are employed (*e.g.* six and fourteen), the percentage of reduction in IGBT numbers substantially falls when compared to HCBs –even when a gradual reduction is still achieved as the number of nodes increases. This occurs as the fault current during a bus fault is higher than the current rating of the ICBs when a new node is connected. Therefore, the MBs of the three ICBs based solutions must include a new string of IGBTs in parallel to increase the current capability to be able to isolate a bus fault. In a protection scheme based on HCBs, adding a new node requires a new breaker; conversely, a new node for ICBs based solutions requires LCSs to be installed only.

Fig. 18 shows the relationship between the rated voltage of the dc network and the number of IGBTs when three nodes are connected. It is observed that either BT-ICB topology requires less IGBTs than HCBs or AS-ICBs. Compared to the use of HCBs, the IGBT count using BT-ICBs can be reduced over 72% when the dc voltage is around 300 kV. Even for the worst case scenario at a dc voltage of 225 kV, a reduction of 45% is achieved. The AS-ICB also reduces the number of IGBTs for a wide range of dc voltages. However, an AS-ICB based solution requires 5% more IGBTs compared to HCBs when the dc voltage is around 225 kV. This is because the MB rating of an AS-ICB is three times larger than that for a single HCB at this voltage level as the current through the MB of an AS-ICB is three times higher. Thus, the total number of IGBTs for the MB of an AS-ICB and for three HCBs is the same. However, the total number of IGBTs in the LCSs of an AS-ICB is larger than that of an HCB as the AS-ICB has one more bypass branch with higher current rating.

Fig. 19 shows the number of IGBTs for different topologies when the terminal inductance is changed. The dc voltage is set to 400 kV and it is assumed that there are three dc nodes. As it can be observed, the use of HCBs requires the highest number of IGBTs. However, the use of larger terminal inductors can reduce the semiconductor device count for all approaches.

It can be concluded from the studies in this section that the BT-ICB$_{type1}$ contains the least number of IGBTs. BT-ICB $_{type2}$ has a slightly greater number of devices due to its additional bypass branches, but the IGBT count is still much lower compared to that of AS-ICBs and HCBs. Both BT-ICBs could be cost-effective alternatives for fully protecting HVDC grids.

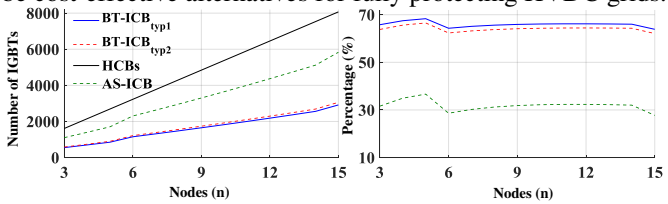



Fig. 17. Impact of the number of nodes on the number of IGBTs.

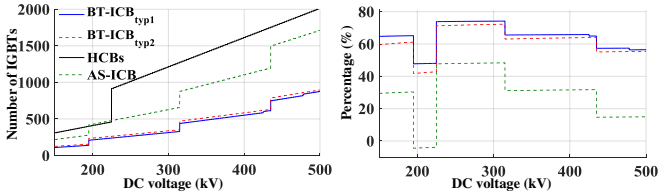



Fig. 18. Impact of the rated dc voltage on the number of IGBTs.

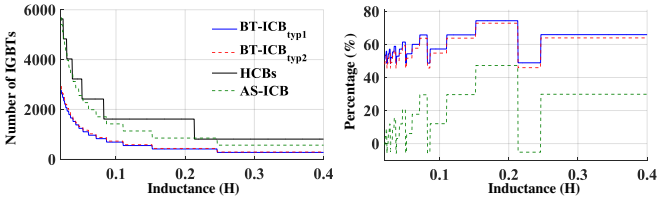



Fig. 19. Impact of the terminal inductance on the number of IGBTs.

### C. *Conduction losses of DCCB topologies*

Consider a three-node circuit breaker (or three HCBs) as an example. The equivalent circuits when conventional HCBs, BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ are employed are given in Fig. 20. The equivalent circuits consist of the bypass branches of DCCBs only as the MBs are bypassed in a no-fault condition. When there is no fault, the MBs are naturally bypassed as they have significantly more semiconductor devices compared to the LCSs in the bypass branches and, thus, incur larger forward voltage drops and exhibit a higher resistance across their terminals. Therefore, the MBs can be considered as open circuits during a non-faulted operating condition, with the bypass branches conducting the current instead.

The bypass branches of HCBs form a star (Y) circuit, while those of BT-ICB$_{typ1}$ constitute a delta ($\Delta$) circuit and those of BT-ICB$_{typ2}$ a Wheatstone circuit.

The on-state resistance $R_{bb}$ and forward voltage drop $U_{bb}$ of a single bypass branch for both BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ will be approximately 1.5 times larger than for a HCB. This is because the bridge-type LCSs of a BT-ICB$_{typ1}$ or a BT-ICB$_{typ2}$ will have 1.5 more semiconductors on their current paths when compared to the anti-series connected circuits used in the LCSs of HCBs (this can be seen in Fig. 20). However, the total power losses of BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ can still be lower than the power losses of HCBs. This occurs since a delta or a Wheatstone circuit can better split the current flow and, hence, reduce the magnitude of current at each bypass branch (this is similar to comparing circuits connected in series and parallel, where a paralleled circuit also splits the current).

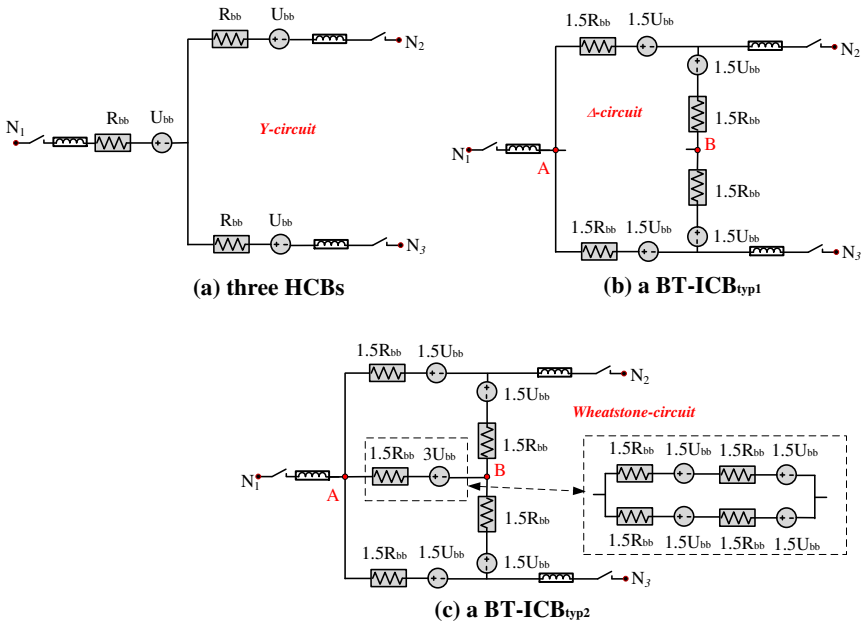



Fig. 20. Equivalent circuits of different DCCBs.

To verify the previous discussion, a simulation is carried out to compare the conduction losses for the three different DCCBs. For simplicity, node $N_1$ is connected to a 400 kV dc voltage source, while $N_2$ and $N_3$ are connected to −1.5 kA and −0.5 kA current sources, respectively. The power at $N_1$ will then be 800 MW. $U_{bb}$ and $R_{bb}$ are selected as 2.1 V and 0.004 Ω, respectively. Results are shown in Fig. 21. As it can be observed, the losses for BT-ICB$_{typ1}$ are 0.043 MW, whereas the losses for BT-ICB$_{typ2}$ 0.04 MW. These values are much lower than those for the HCBs, which stand at 0.069 MW. The losses incurred by BT-ICB$_{typ2}$ are the lowest as this topology has more bypass branches to split the current flow. This can also be seen in Fig. 20(c), where BT-ICB$_{typ2}$ has additional bypass branches connected between Nodes A and B compared to BT-ICB$_{typ1}$ (see Fig. 20(b)). Therefore, the current flowing through BT-ICB$_{typ2}$ is split in a different way than that of BT-ICB$_{typ1}$. As a result, the losses of two BT-ICBs configurations are different, with those of BT-ICB$_{typ2}$ being lower.

It can be concluded from the previous analysis that an additional advantage of using BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ is to reduce the overall conduction losses. This will further increase the cost savings, adding to the benefits of having a reduced number of IGBTs. However, the cost saving afforded by the reduction of conduction losses may not be significant as the losses incurred when using HCBs is already low. For the example presented in this section, the conduction losses when HCBs are employed are 0.069 MW for a power delivery at $N_1$ of 800 MW (0.0086%).

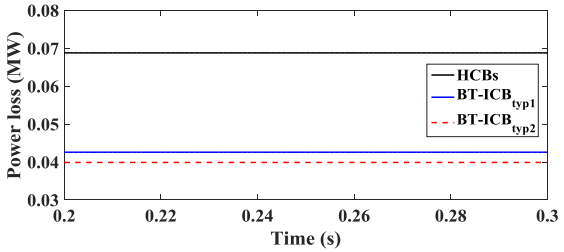



Fig. 21. Comparison of conduction losses.

### D. *Analysis of cost and volume of different DCCBs*

Although there is no data available in the open literature showing the cost of components of DCCBs, it is widely accepted that the semiconductor based MBs incur the highest cost. For example, in [39], [40], the cost of an HCB is evaluated based on the MB only, with the cost of UFDs or even LCSs being ignored. In [39], the cost of a conventional HCB rated at 1500 MW is evaluated to be 12.5 million Euro. In [40], two dc switchyards are compared. One considers a higher number of MBs, while the other features more LCSs and UFDs. It is shown that the cost of the dc switchyard with a higher number of LCSs and UFDs is still the lowest due to the reduction in MBs.

A sensitivity study is performed to evaluate and compare the cost of five different DCCBs. The following devices are considered: BT-ICB$_{typ1}$, BT-ICB$_{typ2}$, HCB, AS-ICB as proposed in [33], and interlink DCCB (denoted Inter-DCCB) as proposed in [30]. The analysis considers the UFDs and IGBTs associated with diodes. The total cost of a DCCB will be the sum of the cost of each component times its number. It is assumed that the contribution of the cooling system towards cost is negligible and hence it is not considered. The rationale for this assumption is that the power losses for BT-ICBs are lower than for conventional HCBs, power losses are low in general for DCCB applications [39], and even the cost of a cooling system for a modular multilevel converter station is limited [41].

The number count of IGBTs in BT-ICB$_{typ1}$, BT-ICB$_{typ2}$, HCBs, and AS-ICB has been provided in Section III-B. The number of IGBTs of an inter-DCCB ($M_{IGBT,inter}$) can be calculated using a similar approach:

$$M_{IGBT,inter} = \sum_{\beta=1}^{n}\left[\text{ceil}\left(\frac{I_{MB,inter\beta}}{I_{igbt}}\right)\times \text{ceil}\left(\frac{1.5U_{rated}}{U_{igbt}}\right)+ 2\text{ceil}\left(\frac{I_{MB,inter\beta}}{I_{igbt}}\right)\times \text{ceil}\left(\frac{U_{\text{LCS},inter\beta}}{U_{igbt}}\right)\right] \quad (29)$$

where $I_{MB,inter\beta}$ is the peak current flowing through the MB of an interlink DCCB and $U_{\text{LCS},inter\beta}$ is the maximum voltage across its LCSs. The number of diodes is proportional to the number of IGBTs; *e.g.* the bridged circuit will have four diodes

for each IGBT and the anti-series circuit will have one diode per IGBT. The number of UFDs in different DCCBs is given in Table II.

TABLE II. NUMBER OF UFDS INCLUDED IN DIFFERENT DCCBS WITH N CONNECTED NODES.

| | BT-ICB$_{typ1}$ | BT-ICB$_{typ2}$ | HCBs | AS-ICB | Inter-DCCB |
|---|---|---|---|---|---|
| No. of UFDs | $2\times(n-1)$ | $2\times(n+1)$ | $n$ | $2\times(n-1)$ | $n$ |

The cost of a single IGBT is assumed to be $C_{IGBT}$. The cost of a diode is $0.1C_{IGBT}$ (10 times less [35]). Let the cost of a UFD be $C_{UFD}$ and the cost of an IGBT $C_{IGBT}$. A weighting factor $k$ is used to relate $C_{UFD}$ with $C_{IGBT}$ as $k = C_{UFD}/C_{IGBT}$. For example, if $k = 5$, the cost of a UFD would be five times of the cost of an IGBT. For this study, the number of connected nodes $n$ is selected as three and $k$ is varied from 5 to 120 (in steps of 0.1). Given that the cost of a UFD may be significantly lower compared to that of the MBs (which could have more than a hundred IGBTs [18], [39]), the value of $k$ should be small and will be likely located in the range between 5 and 120. Such a range will be sufficient to show all the break-even points in terms of cost for the different DCCBs considered in this study.

The comparison results are given in Fig. 22(a). It is observed that the cost of BT-ICB$_{typ2}$ will be the lowest if $k < 45.8$. Given that the BT-ICB$_{typ2}$ topology replaces more semiconductors with UFDs, the less the UFD's cost is, the cheaper BT-ICB$_{typ2}$ will be. If $45.8 < k < 79.5$, BT-ICB$_{typ1}$ is the cheapest; however, when $k > 79.5$ Inter-DCCB becomes the most economic as it has less UFDs than BT-ICB$_{typ1}$ (see Table II). Only if $k$ rises to 89.8 and 105.8, respectively, the cost of BT-ICB$_{typ2}$ and BT-ICB$_{typ1}$ will be higher than when conventional HCBs are used. In addition, the cost the presented BT-ICB topologies will always be lower than the AS-ICB when $k < 120$.

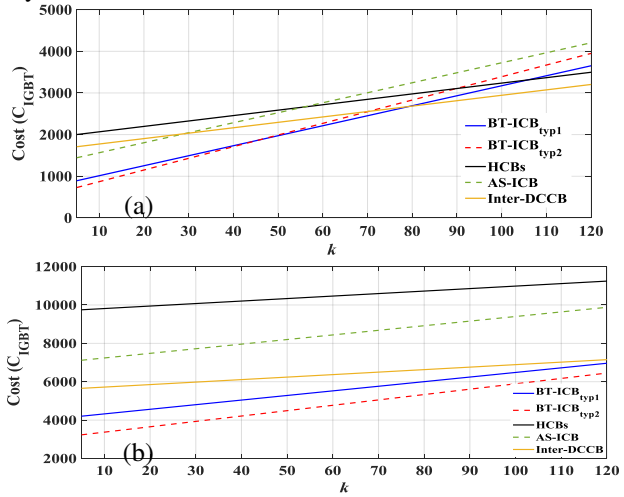



Fig. 22. Cost of different DCCBs with $k$ varied from 5 to 120: (a), with 3 nodes; (b) with 15 nodes.

It is worth mentioning that the cost of a UFD should be considerably less than $100C_{IGBT}$ in practice. Only the MB of a DCCB may require 100 IGBT units to withstand the system voltage. As the cost of the MB is high, this makes the cost of UFDs to be negligible, as previously discussed. Therefore, in practice, $k$ should be reasonably small, making of the proposed BT-ICB topologies good alternatives to reduce costs. Among the two BT-ICB configurations, if $k < 45.8$, BT-ICB$_{typ2}$ is recommended, while if $45.8 < k < 79.5$, BT-ICB$_{typ1}$ could be used.

It should be also noted that the total savings when BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ are employed would increase as the number of connected nodes increases. Fig. 22(b) shows a comparison of the cost of DCCBs when $n = 15$. It can be observed that BT-ICB$_{typ2}$ remains the most economical solution when $k$ varies from 5 to 120—followed by BT-ICB$_{typ1}$.

It should be highlighted that, to the knowledge of the authors, there are no references available in the open literature directly presenting the volume of each component within a DCCB. Reference [40] is relevant as it indicates that the volume of a DCCB can be slightly decreased if the number of MBs is reduced by adding more UFDs. Having said that, the volume in a high voltage system will be dominated by the insulation distance between components instead of their cumulative physical volume. For a DCCB installed in a switchyard or a substation, the insulation distance will be determined not only by the voltage rating of the DCCB, but also by other factors such as the methods and materials used for the insulation. However, a detailed study considering insulation distances requires a deeper analysis and the design of a full structure layout of a switchyard, which falls out of the scope of this paper.

A sensitivity study was undertaken to show how the semiconductor count will affect the volume of DCCB topologies without considering insulation distances. It is assumed that the volume of the MB of a conventional HCB is given by $V_{LMB}$ (which considers two IGBTs and two diodes per anti-series connected circuit). Based on the number of semiconductor devices, the volume of the MBs of BT-ICB$_{typ1}$, BT-ICB$_{typ2}$, AS-ICB and Inter-DCCB would be, respectively, $1.25V_{LMB}$, $0.25V_{LMB}$, $V_{LMB}$ and $0.5V_{LMB}$. The volume of a UFD is assumed to be $d\times V_{LMB}$, where $d$ is a weighting factor relating the volume of a UFD with the volume of the MB of an HCB. Suitable information related to this sensitivity study is summarized in Table III. It should be noticed that the volume of the cooling system is not considered in this study. As the LCSs exhibit significantly fewer IGBTs compared to the MB, their physical volume will be much smaller. Given that the volume of the cooling system is even smaller than that of an LCS [42], no further discussion is warranted.

TABLE III. VOLUME OF DIFFERENT DCCBS WITH N CONNECTED NODES.

| | BT-ICB$_{typ1}$ | BT-ICB$_{typ2}$ | HCBs | AS-ICB | Inter-DCCB |
|---|---|---|---|---|---|
| Volume | $[2d\times(n-1)+1.25]\times V_{LMB}$ | $[2d\times(n+1)+0.5]\times V_{LMB}$ | $n(1+d)\times V_{LMB}$ | $[2d\times(n-1)+1]\times V_{LMB}$ | $[(d+0.5)\times n+1]\times V_{LMB}$ |

Fig. 23(a) shows the volume of different DCCBs when $d$ varied from 0.1 to 1. For simplicity, the number of connected nodes $n$ is selected as 3. It can be seen that if $d = 0.1$ (implying that the volume of a UFD is 10 times less than that of an MB), BT-ICB$_{typ2}$ exhibits the smallest volume as it has the least number of semiconductors. However, since BT-ICB$_{typ2}$ has more UFDs than other DCCB topologies, its volume will increase quickly as $d$ increases. When $d > 0.5$, BT-ICB$_{typ2}$ has the biggest volume. On the other hand, both BT-ICB$_{typ1}$ and AS-ICB have smaller volumes compared to other DCCBs when $0.19 < d < 1$, although the rate of increase in volume is also higher than that for HCBs and Inter-DCCBs.

If $n = 15$, BT-ICB$_{typ1}$ BT-ICB$_{typ2}$ and AS-ICB will have similar volumes. When $d < 0.45$, these topologies will have a smaller volume as they feature considerably less

semiconductors. Only if $d > 0.55$, the Inter-DCCB will have the smallest volume as it has less UFDs than BT-ICB$_{typ1}$, BT-ICB$_{typ2}$ and AS-ICB, as well as less semiconductors than HCB. However, considering that BT-ICB$_{typ1}$ and BT-ICB$_{typ2}$ can significantly reduce cost as shown in Fig. 22, these two DCCBs arguably render the most cost-effective solutions.

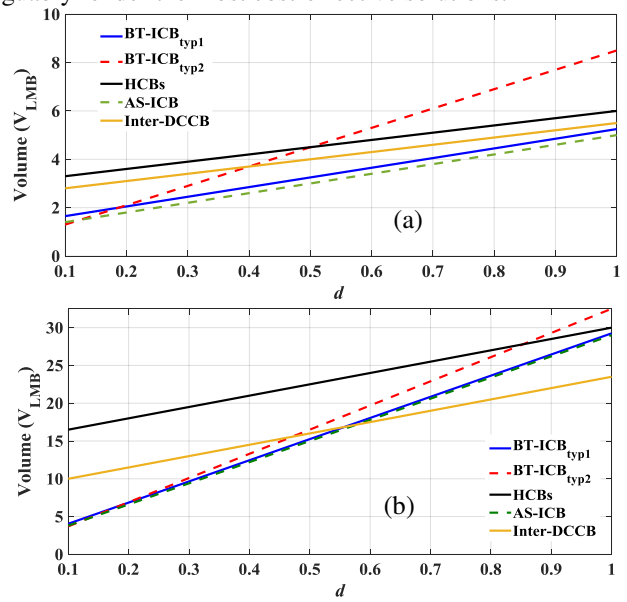



Fig. 23. Volume of different DCCBs with $d$ varied from 0.1 to 1: (a), with 3 nodes; (b) with 15 nodes.

When directly comparing BT-ICB topologies, BT-ICB$_{typ2}$ will incur less cost for a small value of $k$, while BT-ICB$_{typ1}$ will feature a relatively smaller volume. Therefore, BT-ICB$_{typ2}$ could be more suitable for onshore HVDC applications where space may not be a critical issue, while BT-ICB$_{typ1}$ would be better suited offshore, as the cost of an offshore platform is already very high, and thus, smaller volumes in any components are preferred.

### *E. Impact of surge arresters in cost and volume of different DCCBs*

Surge arresters may also affect the cost and volume of a DCCB. The necessary number of surge arresters is mainly determined by the required voltage and energy rating of the MB—multiple surge arresters need to be connected in series to reach a certain voltage and energy level, and then connected in parallel with the MBs. Therefore, if the voltage and energy rating of different DCCBs is similar, the number of surge arresters connected in parallel with their MBs will be also the same. However, it should be borne in mind that the presented BT-ICB configurations have a single MB shared between different nodes, while conventional HCBs consider one MB at each node; therefore, a BT-ICB requires less surge arresters.

The impact in cost and volume can be further reduced as the number of connected nodes increases. Using this rationale, the more expensive the surge arresters are, the least overall cost is incurred in total when adopting the presented BT-ICBs configurations instead of other alternatives. A similar argument can be drawn for volume: the larger the surge arresters are, the least effect in the total volume they will contribute for a BT-ICB topology as opposed to other DCCB configurations.

A simple counting exercise is carried out to estimate the number of surge arresters for the different DCCB topologies mentioned in Section III-D. For simplicity, it is assumed that the number of surge arresters needed for one MB is $n_{sa}$ and that the number of nodes is $n$. For the BT-ICBs and AS-ICB topologies, the total number will be $n_{sa}$ as they all share one MB. This number will increase to $n_{sa} \times n$ for conventional HCBs and to $0.5\ n_{sa} \times n$ for the inter-DCCB configuration as the number of required MBs for these topologies increases with the number of nodes. However, as the inter-DCCB uses only half of a MB per node, the number of required surge arresters is in turn half when compared to an HCB.

Although the previous discussion suggests that the presented BT-ICBs and the AS-ICB will be the least affected configurations in terms of cost and volume when surge arresters are considered, a more detailed study is necessary to fully support this observation. Such a study falls out of the scope of this work.

## IV. Simulation Studies

### *A. Test System*

A dc protection scheme using BT-ICBs is assessed in the 400 kV four-terminal HVDC system shown in Fig. 24. The DCCBs ($CB_1$ to $CB_4$) are located at each end of the overhead lines (OHLs) and are either BT-ICB$_{typ1}$ or BT-ICB$_{typ2}$ (see Section IV-C). The current convention is given in Fig. 25. The ac systems are rated at 230 kV. $MMC_1$ regulates dc voltage to 400 kV, while $MMC_2$, $MMC_3$ and $MMC_4$ operate in power control mode to regulate power to 200, −200 and 200 MW.

### *B. Modeling of DC Components*

All DCCBs are modeled as either BT-ICB$_{type1}$ or BT-ICB$_{type2}$. The LCSs and BTMBs are modeled based on the data of 5SNA 3000K452300. The rating of LCSs and BTMBs is selected using the analysis from Section III. If BT-ICB$_{type1}$ is used, a reduction of 60.05% of IGBTs (966) is achieved compared to the use of HCBs (2448). Conversely, the reduction is 57.73% for BT-ICB$_{type2}$ (1034). The UFDs are modeled as mechanical switches with an operation delay of 2 ms. The CLRs are set to 0.05 H and surge arresters are rated at 1.5 p.u.

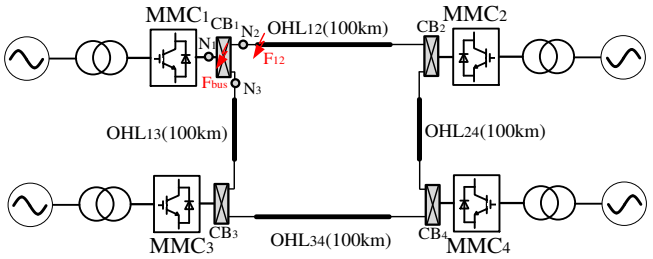



Fig. 24. One-line diagram of the meshed dc test system.

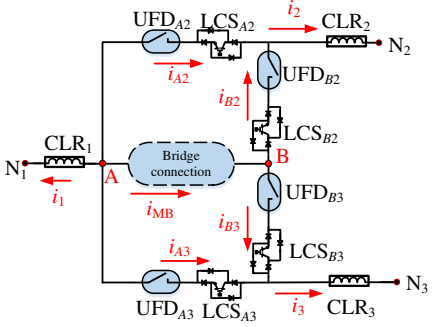



Fig. 25. Current convention of BT-ICBs.

All OHLs are represented using the frequency dependent model available in PSCAD. The conductor (type AAAC-806-

A4-61) and ground wire (type AFL CC-75-528) data for the OHL model can be found in [43], [44]. The structure of the tower is provided in [45]. All MMCs are represented as Thévenin equivalent models [46].

### C. Case Studies

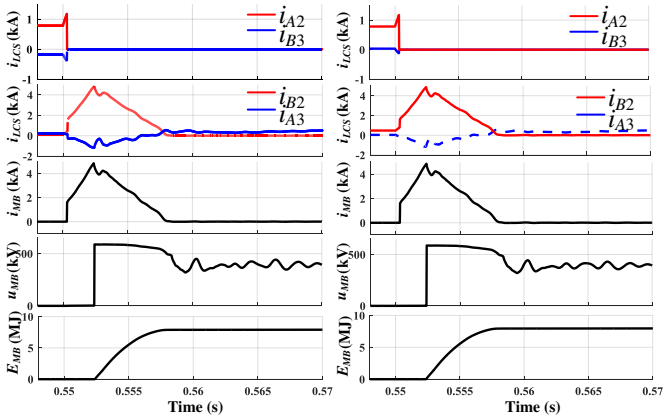
Two studies are performed:

- Study 1: a solid fault ($F_{12}$) at the end of $OHL_{12}$ at 0.55 s;
- Study 2: a solid fault at bus B ($F_{bus}$) of $CB_{21}$ at 0.55 s.

In Study 1, the fault is detected at $CB_{12}$ and $CB_{21}$ and the DCCBs start to operate following the sequence established in Section II. Due to space limitations, only measurements at $CB_{12}$ are provided. Fig. 26(a) shows the simulation results when all DCCBs are BT-$ICB_{typ1}$. Once the fault is detected, $LCS_{A2}$ and $LCS_{B3}$ will immediately open and their currents ($i_{A2}$ and $i_{B3}$) drop to zero. The UFDs associated with $LCS_{A2}$ and $LCS_{B3}$ will incur a delay of 2 ms to fully open. The currents in $LCS_{B2}$ ($i_{B2}$), $LCS_{A3}$ ($i_{A3}$) and the BTMB ($i_{MB}$) keep increasing during this time. Current $i_{B2}$ remains similar to $i_{MB}$ since $LCS_{B2}$ is in series with the BTMB after $LCS_{A2}$ and $LCS_{B3}$ open. Both $i_{B2}$ and $i_{MB}$ increase to a peak value of 4.859 kA before being interrupted by the BTMB. After the interruption, $i_{B2}$ and $i_{MB}$ drop to zero and the fault energy (about 7.5 MJ) is absorbed by the surge arresters. The fault is then isolated. The maximum voltage across the BTMB is 600 kV, which is determined by the rating of the surge arresters (1.5 p.u.). The current is still transmitted between the healthy nodes as $i_{A3}$ is not zero.

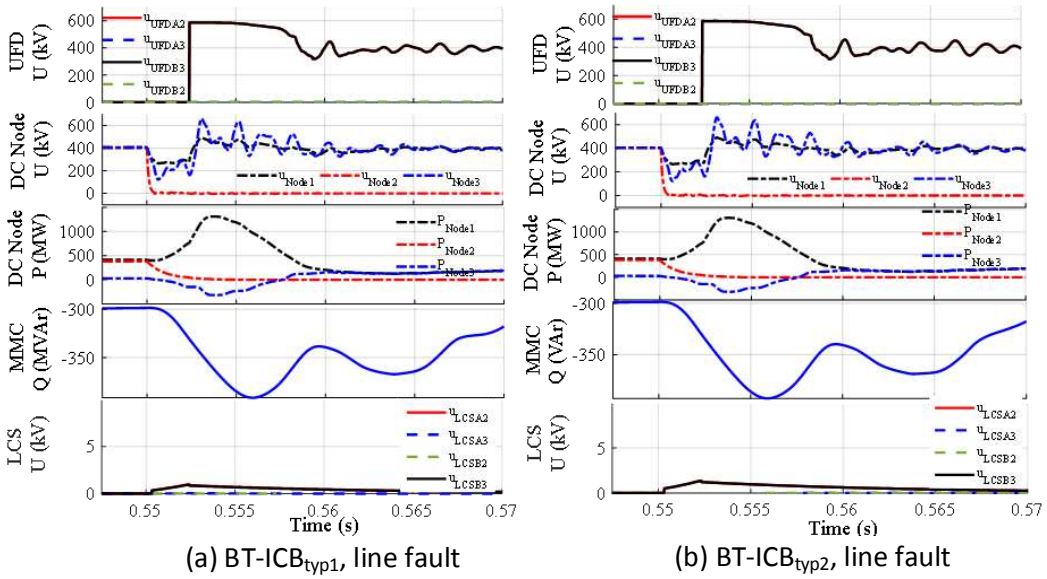
Fig. 26(b) shows the results when BT-$ICB_{typ2}$ is used instead. $LCS_{A2}$, $LCS_{B3}$, and the extra bypass branches in the backward direction first open when the fault is detected. Currents then increase in the other LCSs and the BTMB. The peak current before interruption is 4.87 kA (almost the same as when BT-$ICB_{typ1}$ are used). After the interruption, the current of BTMB drops to zero and the healthy nodes keep transmitting current.

Fig. 27 shows the UFD voltages, node voltages, node active power, MMC reactive power and LCS voltages when BT-$ICB_{typ1}$ or BT-$ICB_{typ2}$ acts to block the line fault. Both BT-ICBs exhibit similar dynamics. It can be observed that the opened UFD ($UFD_{A2}$) also needs to withstand a maximum dc voltage of ≈600 kV—similar to the dc voltage of the BTMB. All opened UFDs exhibit identical voltages following the fault event. The UFD that remains closed ($UFD_{A3}$) has a zero voltage. The voltage across opened LCSs is extremely small (less than 2 kV). This is expected as the opened UFDs withstand the dc voltage (≈600 kV) and hence the LCS voltages are negligible in comparison. The dc voltages at the three nodes drop before the fault is blocked. The voltage at the faulty line ($u_{node2}$) drops to zero directly while the voltages at nodes $N_1$ and $N_3$ ($u_{node1}$ and $u_{node3}$) stay to a higher value due to the existence of reactors between $N_1$, $N_3$ and the faulty line. Once the fault is blocked, $u_{node1}$ and $u_{node3}$ start to recover to 400 kV. The magnitudes of power at $N_1$ ($P_{node1}$), $N_2$ ($P_{node2}$) and $N_3$ ($P_{node3}$) prior to the fault are 414 MW, 384 MW and 30 MW, respectively. After the fault, $P_{node2}$ becomes zero due to fault isolation and power is only transmitted between $N_1$ and $N_3$. Note $N_1$ is connected to converter; hence the active power of MMC1 is the same as $P_{node1}$. The reactive power of MMC1 is slightly influenced by the dc fault, but it starts to recover once the fault is blocked.



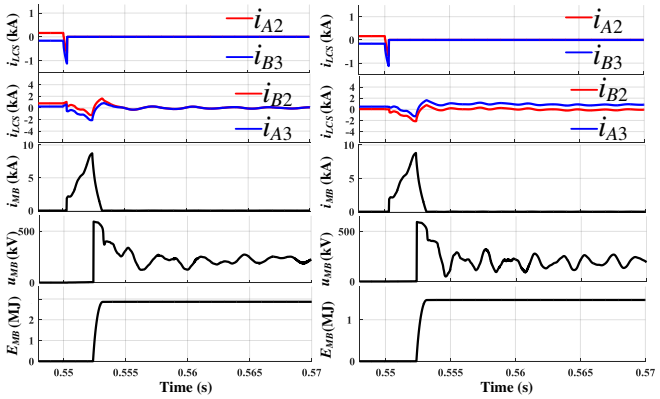

(a) BT-$ICB_{typ1}$, line fault (b) BT-$ICB_{typ2}$, line fault

Fig. 26. Results for Study 1. Protection using (a): BT-$ICB_{typ1}$; (b): BT-$ICB_{typ2}$.




(a) BT-$ICB_{typ1}$, line fault (b) BT-$ICB_{typ2}$, line fault

Fig. 27. UFD voltages, node voltages, node power, MMC reactive power and LCS voltages in Study 1: (a) BT-$ICB_{typ1}$; (b) BT-$ICB_{typ2}$.




(a) BT-ICB$_{typ1}$, bus B fault (b) BT-ICB$_{typ2}$, bus B fault

Fig. 28. Results for Study 2. Protection using (a): BT-ICB$_{typ1}$; (b): BT-ICB$_{typ2}$.

In Study 2, the bus fault is immediately detected at CB$_{12}$. Fig. 28(a) shows results when a BT-ICB$_{typ1}$ is employed to isolate the fault at bus B. BT-ICB$_{typ1}$ first turns off LCS$_{B2}$ and LCS$_{B3}$ and then waits until the corresponding UFDs open to, in turn, open its BTMB. The peak current flowing through the BTMB reaches 8.73 kA prior to the interruption, which is larger than that for a dc line fault (as expected). However, the current drops much faster after the interruption and this leads to less absorbed energy (≈1.5 MJ). This occurs since the equivalent terminal inductance for a bus fault is smaller than that for a dc line fault (*i.e.* $L_{hlthyB} < (L_{hlthy} + L_j)$) as mentioned in Section III and, hence, there is less energy stored in these reactors. Currents are still transmitted through the nodes despite of the bus fault.

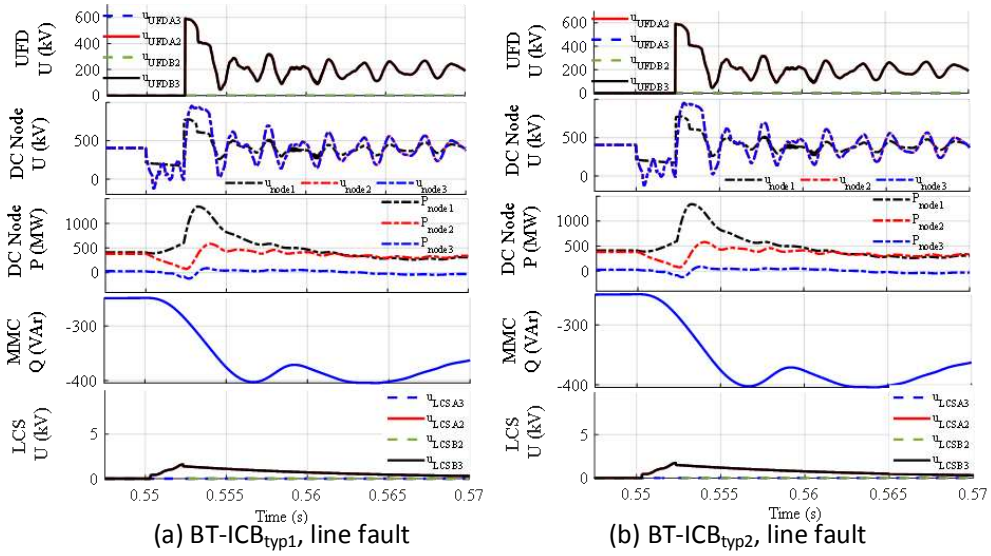
Fig. 28(b) shows results when BT-ICB$_{typ2}$ is used. As it can be observed, the fault can be also successfully isolated. The dynamics of the currents when BT-ICB$_{typ2}$ is employed are similar to those when BT-ICB$_{typ1}$ is used.

Fig. 29 shows the UFD voltages, node voltages, node active power, MMC reactive power and LCS voltages when BT-ICB$_{typ1}$ or BT-ICB$_{typ2}$ acts to block the bus fault. The dynamics of both topologies are similar. As in Study 1, the opened UFD needs to withstand a maximum dc voltage of 600 kV and the LCS voltages are negligible in comparison. However, the oscillation of the dc node voltages and power during this type of fault are more significant than for a dc line fault since a bus fault current is larger than a dc line fault current. After the fault is blocked, the fault current quickly drops to zero and an initial dc voltage overshoot is present due to the inductive components of the dc system. The subsequent oscillations in the dc node voltage (and thus, power) are mainly caused by the charging and discharging of the inductive and capacitive components of the system's overhead lines. Since the overhead lines have small capacitances and large inductances, these voltage oscillations are hence large.

In addition, the three nodes keep transmitting power once the bus fault is successfully isolated. The reactive power of MMC$_1$ is slightly more affected during a dc bus fault than for a dc line fault – although arguably the influence is still small.

For completeness, an additional test is carried out to compare the protection performance between the proposed BT-ICBs and HCBs. To be able to carry out this, three HCBs are required to replace a single BT-ICB, as shown in Fig. 30. The same line fault for Study 1 is applied at the end of OHL12 (N$_2$) at 0.55 s. The HCB connected to N$_2$ will open to block the fault. Simulation results are given in Fig. 31, showing the voltages and currents of the opened HCB connected to N$_2$, the node voltages, power and reactive power of MMC$_1$. The HCBs connected to N$_1$ and N$_3$ remain closed and hence further discussion on these devices is omitted.

The results in Fig. 31 show that the voltage and current exhibited by the HCB are similar to those of either BT-ICB topology (see Figs. 26 and 27). The current flowing through the LCS ($i_{LCSHCB}$) reaches 1.6 kA before it opens to commutate the fault current to the MB. This is slightly higher than $i_{A2}$ and $i_{B3}$ for the BT-ICBs as multiple bypass branches split the current flow. The peak current flowing through the MB of the HCB ($i_{MBSHCB}$) reaches 4.79 kA, which is close to that of the BT-ICBs (around 4.85 kA). Similarly, after the MB of the HCB is opened, the voltages across the MB and the UFD are almost identical, with both reaching around 600 kV. The voltage of the LCS is negligible—less than 2 kV only as the UFD withstands the dc voltage. The energy absorbed is around 6.4 MJ, which is slighter lower than that of BT-ICBs. The voltage and power at each node are also similar to those exhibited by the BT-ICBs when used. These become zero at N$_2$ after the fault is




(a) BT-ICB$_{typ1}$, line fault (b) BT-ICB$_{typ2}$, line fault

Fig. 29. UFD voltages, node voltages, node power, MMC reactive power and LCS voltages in Study 2: (a) BT-ICB$_{typ1}$; (b) BT-ICB$_{typ2}$.

interrupted, while the power and voltages at the healthy circuits ($N_1$ and $N_3$) start to recover following fault interruption. The reactive power is slightly affected in the same way as when BT-ICBs are used—dropping to around −340 MVAr before it starts to recover. These results are meaningful and show that the performance afforded by the proposed BT-ICBs is consistent with that of an HCB.

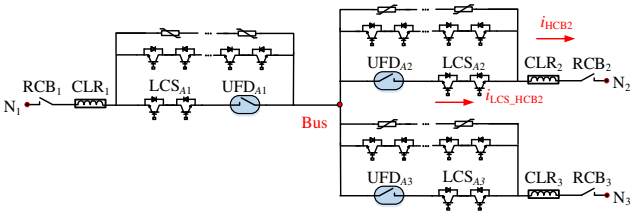



Fig. 30. Replacement of a BT-ICB with three HCBs.

It should be emphasized that Study 2 cannot be recreated when HCBs are employed as bus B does not exist. Instead, this would be replaced by a single common bus, as shown in Fig. 30. Should a fault happen at the common bus, all three HCBs should open to isolate the common bus fault and, as a result, power transmission would be interrupted among $N_1$, $N_2$ and $N_3$. This is a significant disadvantage compared to the BT-ICB configurations. As shown by the results in Figs. 28 and 29, power can still be transmitted if BT-ICBs are used. More importantly, given that $N_1$ is connected to $MMC_1$ which, in turn, regulates the dc voltage of the system, if an HCB connected to $N_1$ opens the dc voltage would become unregulated and the entire dc system would collapse. Although this could be avoided if another MMC changes from power to dc voltage control mode during the fault event, this may increase the burden in the control requirements of the dc system.

## V. Conclusion

This paper proposes the use of two different BT-ICBs for HVDC grid protection. Both topologies have one shared BTMBs associated with several bypass branches and, hence, reduce considerably the required number of controllable semiconductor devices. Moreover, the BT-ICBs can protect a dc network from faults at various locations of the dc grid, including dc lines, converter terminals and dc buses. A distinctive advantage of the presented BT-ICB configurations is that the current flowing within healthy circuits will not be blocked even during a dc bus fault event. Conversely, when conventional topologies are employed, all HCBs linked to the faulty bus will trip and the current from healthy circuits will be blocked as well.

An adequate coordinated operation principle of both BT-ICBs has been established. A mathematical framework is provided to analyze the impact that different parameters and components have in the design of each topology. Detailed sensitivity studies have been undertaken to assess their advantages over other alternatives. Compared to DCCB configurations reported in the literature, the proposed BT-ICB topologies significantly reduce the use of controllable semiconductor devices. Moreover, the cost of the proposed BT-ICBs when compared to other DCCB topologies will be reduced and such a reduction will be more significant as the number of connected nodes increases. Although the volume of the BT-ICBs will be in turn dependent on the volume of its UFDs, it should be borne in mind that the insulation distances and not the cumulative volume of the physical components will dictate the overall volume of a high voltage system. However, based on the analyses presented in the paper, the proposed BT-ICB configurations have the potential to be highly competitive in HVDC applications.

Both BT-ICBs configurations have been simulated in PSCAD using a four-terminal HVDC grid. The results show the effectiveness of using the BT-ICBs to isolate both dc line and internal bus faults.

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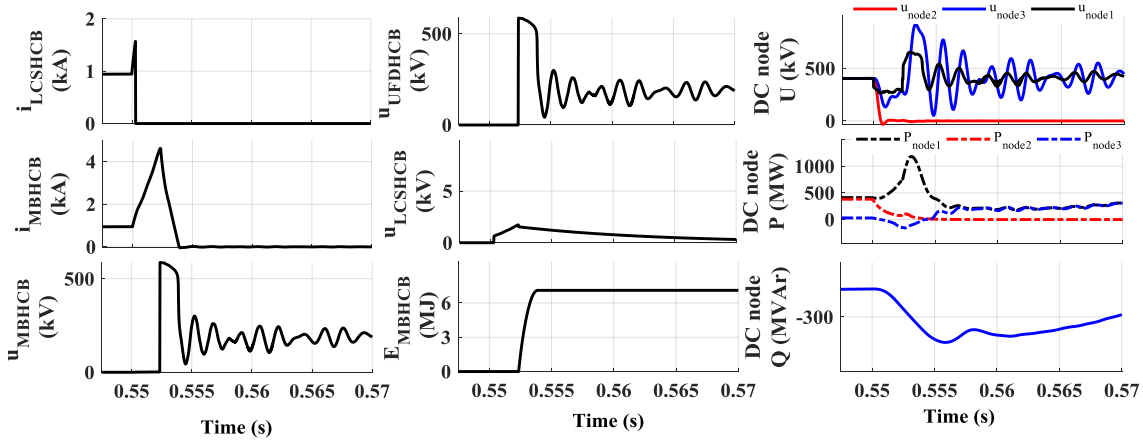


Fig. 31. Simulation results for an HCB (Study 1).

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